IN THE CLAIMS:

1. (Currently Amended) A data recovery apparatus, comprising:

a phase locked loop (PLL) for generating a plurality of phase clock signals each having a different delay time with respect to a clock signal;

an oversampler for M times oversampling serial input data in response to the plurality of phase clock signals and outputting a plurality of data bits in parallel;

a level transition detector for receiving the parallel data bits output from the oversampler, detecting logic level transitions between successive bits ~~the point of time at which the logic level transitions between adjacent ones~~ of the parallel data bits and ~~outputting the~~ generating a detection result as one of M transition signals ~~as first through Mth transition signals~~;

a transition accumulator for accumulating ~~the~~ a number of times each one of the ~~first through Mth~~ M transition signals is generated and outputting ~~one of~~ a transition accumulation signal corresponding to ~~first through Mth transition accumulation signal associated with~~ the transition signal whose generation frequency is highest, the transition accumulation signal comprising one of M transition accumulation signals,

wherein the transition accumulator comprises a reset signal generator for performing a logic combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the transition accumulator in response to the logic combination result;

a state selector for generating a state signal in response to the transition accumulation signal output from the transition accumulator, wherein the state signal is used for selecting data bits of corresponding positions among the parallel data bits output from the oversampler; and

a data selector for receiving the parallel data bits, utilizing the state signal to select from the parallel data bits those data bits having sampling positions corresponding to the state of the state signal, and outputting the selected data bits in parallel.

2. (Original) The data recovery apparatus of claim 1, wherein M is 3.

3. (Currently Amended) The data recovery apparatus of claim 2, wherein the level transition detector comprises:

a transition detector comprising a plurality of exclusive OR gates for performing an exclusive OR operation on two adjacent bits of the paralled data bits output from the oversampler and generating exclusive OR results as first, second, and third output signals; and

a transition detection signal outputting unit for processing the first, second, and third output signals to generate and output a first, second or third transition signal as a result of said processing ~~the processing results as the first through third transition signals~~.

4. (Currently Amended) The data recovery apparatus of claim 3, wherein the transition accumulator comprises:

a first accumulator for accumulating the first transition signal in response to ~~the~~ an input clock signal and outputting a first transition accumulation signal ~~at a first level~~ when a predetermined number of first transition signals are accumulated;

a second accumulator for accumulating the second transition signal in response to the input clock signal and outputting a second transition accumulation signal ~~at a first level~~ when a predetermined number of second transition signals are accumulated;

a third accumulator for accumulating the third transition signal in response to the input clock signal and outputting a third transition accumulation signal ~~at a first level~~ when the accumulated number is a predetermined number; and

wherein the ~~a~~ reset signal generator performs the ~~for performing a~~ logic combination on the first, second, and third transition accumulation signals and generates the ~~generating an~~ accumulation reset signal for resetting the first, second, and third accumulators in response to the logic combination result.

5. (Original) The data recovery apparatus of claim 4, wherein the transition accumulator outputs one of the first, second, and third transition signal having the highest generation frequency as a corresponding one of the first, second, and third transition accumulation signals.

6. (Currently Amended) The data recovery apparatus of claim 4, wherein the state signal generated by the state selector comprises a two-bit signal comprising a first and second bit, ~~wherein different combinations of the logic levels of the first and second bits are set based on~~ to indicate which of the first, second and third transition accumulation signals is generated.

7. (Original) The data recovery apparatus of claim 6, wherein the first and second bits are respectively set to logic "0" and "1" when the first transition accumulation signal is generated, logic "1" and "0" when the second transition accumulation signal is generated, and logic "0" and "0" when the third transition accumulation signal is generated.

8. (Currently Amended) The data recovery apparatus of claim 7, wherein the data selector comprises a plurality of multiplexers m(i), wherein each multiplexer receives M bits of the parallel data bits output from the oversampler and selectively outputs one bit among the M bits in response to the state signal.

9. (Currently Amended) The data recovery apparatus of claim 8, wherein ~~when the M-bit data input to the plurality of multiplexers are represented to be 3P, 3P+1, and 3P+2,~~ each multiplexer m(i) (i = 1, 2, 3, 4) receives the M bits of the parallel data bits at bit positions D(p) where p= (3P, 3P+1, 3P+2), where P= i-1, and wherein the data selector outputs the 3P+2th bits output from the plurality of multiplexers m(i) when the state signal is "01", outputs the 3Pth bits output from the plurality of multiplexers m(i) when the state signal is "10", and outputs the 3P+1th bits output from the plurality of multiplexers m(i) when the state signal is "00", ~~wherein P is an integer not less than 0~~.

10. (Currently Amended) A data recovery method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel;

(b) detecting a level transition ~~in a level~~ between successive bits ~~adjacent ones~~ of the N data bits and ~~outputting~~ generating a transition signal when a level transition is detected ~~one~~

~~of a first through Mth transition signals at the point of time of a detected level transition~~, the transition signal comprising one of M transition signals;

(c) accumulating ~~the~~ a number of generations of each of the M ~~first through Mth~~ transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

(d) ~~detecting the transition signal whose generation frequency meets a predefined threshold~~ performing a logic combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating process in response to the logic combination result; and

(e) selecting from the N data bits, K data bits corresponding to the ~~detected~~ transition signal whose generation frequency meets the predefined threshold.

11. (Original) The data recovery method of claim 10, wherein M is 3.

12. (Original) The data recovery method of claim 11, wherein K is 4 and N is 12.

13. (Canceled)

14. (Currently Amended) The data recovery method of claim 11, wherein the N parallel data bits include bits D(i) (i=0, … N-1) in three-times oversampling positions, and wherein step (e) comprises the steps of:

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of a~~ three-times oversampling position (3P+2), for (P=0, … K-1), corresponding to ~~the~~ a first transition signal of the M transition signals when the first transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold;

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of an~~ three times oversampling position (3P), for (P=0, … K-1), corresponding to the second transition signal when the second transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold; and

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of a~~ three times oversampling position (3P+1), for (P=0, … K-1), corresponding to the third transition signal when third transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold.

15. (Currently Amended) The data recovery method of claim 10, wherein step (e) comprises the step of generating a state signal comprising a predetermined value based on the ~~detected~~ transition signal ~~in step (d)~~ whose generation frequency meets the predefined threshold and selecting the N data bits.based on the value of the state signal.

16. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform method steps for recovering data, the method comprising the steps of:

(a) receiving as input serial data in blocks of K bits and performing an M times oversampling on each block of serial data using N phase clock signals having different delay times to output N data bits in parallel;

(b) detecting a level transition ~~in a level~~ between successive bits ~~adjacent ones~~ of the N data bits and ~~outputting~~ generating a transition signal when a level transition is detected ~~one of a first through Mth transition signals at the point of time of a detected level transition~~, the transition signal comprising one of M transition signals;

(c) accumulating ~~the~~ a number of generations of each of the M ~~first through Mth~~ transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

(d) ~~detecting the transition signal whose generation frequency meets a predefined threshold~~ performing a logic combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating process in response to the logic combination result; and

(e) selecting from the N data bits, K data bits corresponding to the ~~detected~~ transition signal whose generation frequency meets the predefined threshold.

17. (Original) The program storage device of claim 16, wherein M is 3.

18. (Canceled)

19. (Currently Amended) The program storage device of claim 17, wherein the N parallel data bits include bits D(i) (i=0, … N-1) in three-times oversampling positions, and wherein the instructions for performing step (e) comprise instructions for performing the steps of:

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of a~~ three-times oversampling position (3P+2), for (P=0, … K-1), corresponding to ~~the~~ a first transition signal of the M transition signals when the first transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold;

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of an~~ three times oversampling position (3P) , for (P=0, … K-1), corresponding to the second transition signal when the second transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold; and

selecting K oversampled data bits from the N parallel data bits at each ~~by one bit of a~~ three times oversampling position (3P+1), for (P=0, … K-1), corresponding to the third transition signal when third transition signal is ~~detected in step (d)~~ the transition signal whose generation frequency meets the predefined threshold.

20. (Currently Amended) The program storage device of claim 16, wherein the instructions for performing step (e) comprise instructions for performing the steps of generating a state signal comprising a predetermined value based on the ~~detected~~ transition signal ~~in step (d)~~ whose generation frequency meets the predefined threshold and selecting the N data bits based on the value of the state signal.

21. (Currently Amended) A circuit for recovering data, the circuit comprising:

a first circuit for performing an M times oversampling on a block of input serial data using N phase clock signals having different delay times and outputting N data bits in parallel;

a second circuit for detecting a level transition ~~in a level~~ between successive bits ~~adjacent ones~~ of the N data bits and ~~outputting~~ generating a transition signal when a level transition is detected ~~one of a first through Mth transition signals at the point of time of a detected level transition~~, the transition signal comprising one of M transition signals;

a third circuit for accumulating ~~the~~ a number of generations of each of the M ~~first through Mth~~ transition signals and outputting a transition accumulation signal corresponding to a transition signal whose generation frequency meets a predefined threshold, the transition accumulation signal comprising one of M transition accumulation signals;

a fourth circuit for ~~detecting the transition signal whose generation frequency meets a predefined threshold~~ performing a logic combination of the M transition accumulation signals and generating an accumulation reset signal for resetting the accumulating process in response to the logic combination result; and

a fifth circuit for selecting from the N data bits, K data bits corresponding to the ~~detected~~ transition signal whose generation frequency meets the predefined threshold.